Page 3, line 14, insert: "SUMMARY OF THE INVENTION".

Page 3, line 34, insert: "CONCISE DESCRIPTION OF THE DRAWINGS".

Page 4, line 17, insert: "DETAILED DESCRIPTION OF THE DRAWINGS".

IN THE CLAIMS:

Please cancel claims 1-4 without prejudice.

Please add new claims 5 and 6 as follows:

--5. (New) An electronic phase-locked loop for the jitter-attenuated generation of a high-frequency output clock signal which is phase-synchronous with respect to a reference clock signal, having:

a digitally controllable oscillator,

a drive circuit,

which digitally sets the output clock signal of the oscillator until a phase error between the output clock signal and a reference clock signal, which is specified discreetly by a counter reading of a counter, is zero,

a digital phase detector,

which compares the output clock signal of the oscillator with the reference clock signal via a PI filter and the drive circuit,

an analog phase detector,

a lock detection circuit for avoiding a phase quantization error, and

activating the analog phase detector if the phase error specified by the counter reading is zero,

the activated analog phase detector regulating the output clock signal of the oscillator in a continuously variable manner until the clock signal edge of the output clock signal and of the reference clock signal are fully synchronous,

the look detection circuit deactivating the analog phase detector and activating the digital phase detector if the phase error between the output clock signal and the reference clock signal exceeds a specific phase error.